IP_SMPTE2059_SLV

The IP_SMPTE2059_SLV of our Video-over-IP core family is a slave IP core conforming to SMPTE ST 2059-1 and -2.

The IP_SMPTE2059 series are composed of 2 types of cores, a master functionality of vPTPM (Master-Core) and a slave functionality of vPTPS (Slave-Core), it can be used with a single, multiple, or combination of cores.

In addition, control packets via bi-directional ports on MPU bus has a capability to implement AMWA-NMOS functionality.

	Features
1.	Compliant to SMPTE 2059-1 and -2
2.	A video clock (148.5 MHz / 148.35 MHz) and video frame timing generation
3.	An audio clock (24.576 MHz) and an audio sample clock (48 MHz) generation
4.	Counter output for PTS
5.	1 PPS output
6.	Serial output for time data
7.	MPU accessibility by sending and receiving control packets
8.	Ethernet port compatible with GbE, 10 GbE, and 25 GbE
9.	Extensibility for time synchronization with hitless with duplicate redundant lines
10.	125 MHz clock recovery with an fPLL inside an FPGA or an external VCXO